CLAIMS

1. A matched filter circuit, characterized by including:

a first sum and product arithmetic unit having: m switches, each connected with a reception signal in parallel and sequentially outputting each of m reception signals (m is a natural number of 2 or more); hold circuits ,each connected to an output of each switch and holding the output of each switch; multipliers, each multiplying the output of each hold circuit by each value circularly supplied of a first sequence of which length is m; and an adder adding outputs of the multipliers; and

a second sum and product arithmetic unit operating the sum of product of each output of the first sum and product arithmetic unit and each value of a second sequence of which length is n (n is a natural number of 2 or more).

2. A matched filter circuit, characterized by including:

a first sum and product arithmetic unit operating the sum of product of each reception signal and each value of a first sequence of which length is m (m is a natural number of 2 or more); and

a second sum and product arithmetic unit having: n hold circuit groups, each sequentially holding and outputting each output of the first sum and product arithmetic unit, and thereby, outputting n signals (n is a natural number of 2 or more) as a whole; multipliers

multiplying the output of each hold circuit by each value circularly supplied of a second sequence of which length is n; and an adder adding outputs of the multipliers.

3. The matched filter circuit according to claim 2, characterized in that each of the hold circuit groups sequentially holds continuous m outputs of the first sum and product arithmetic unit.

4. The matched filter circuit according to claim 2 or 3, characterized in that each of the hold circuit groups includes:

m switches, each connected with the output of the first sum and product arithmetic unit in parallel and sequentially outputting each of m outputs;

hold circuits, each connected to an output of each switch and holding an output of each switch; and

a multiplexer selectively outputting any one of the outputs of the hold circuits.

5. The matched filter circuit according to claim 1, characterized in that the hold circuits are register circuits or memory circuits.

6. The matched filter circuit according to claim 3 or 4, characterized in that each of the hold circuit groups is a memory circuit, and read/write of the memory circuit is carried out in a manner that in m×n cycles, read and write are alternately carried out in m periods, and in m×(n-1) periods other than above, only read is carried out.